Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.050”**

**.050”**

**14 13 12 11 10**

**2 3 4 5 6**

**15**

**16**

**1**

**9**

**8**

**7**

**5998A**

**MASK**

**REF**

**PAD FUNCTION:**

1. **Collector Q1**
2. **Collector Q2**
3. **Base Q2**
4. **Emitter Q2**
5. **Substrate**
6. **Base Q3**
7. **Collector Q3**
8. **Emitter Q3**
9. **Collector Q4**
10. **Base Q4**
11. **Emitter Q4**
12. **Emitter Q5**
13. **Base Q5**
14. **Collector Q5**
15. **Emitter Q1**
16. **Base Q1**

**NOTE: The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 5998A**

**APPROVED BY: DK DIE SIZE .050” X .050” DATE: 7/13/22**

**MFG: RCA/HARRIS THICKNESS .020” P/N: CA3183**

**DG 10.1.2**

#### Rev B, 7/1